Potentiometric and Transimpedance Amplifiers for Bioelectric signals Analysis and Implementation

Introduction

Bioelectric signals need to be measured for a variety of applications, most notably in healthcare and research. While such signals are predominantly on the lower frequency ranges, they often have very small amplitudes. For example, amperometric sensors often produce currents in the sub-picoamp range. As such, minimizing noise pick-up and high gain are of vital importance. Additionally, it is worth noting that bioelectric sensors often have exceptionally high impedance (potentiometric sensors often have resistances in the order of 10s of GOhms).

The above specifications, as well as the importance of high accuracy biomedical readings, make designing instruments to measure bioelectric signals, challenging. However, all designs can, in broad terms, be described by:

a. The analog front end (AFE) which is responsible for interfacing with the sensor, amplifying the signal and filtering noise,
b. the digital stage is responsible for quantizing (ADC) and transmitting the signal,
c. a power supply.

The goal of this report is to design a device that can measure signals of a range of amplitudes from biological and chemical sensors. To achieve this, we will:

1. Discuss the errors arising when interfacing an amplifier with high impedance voltage sensors;
2. Design two amplifiers for use with potentiometric sensors;
3. Design and analyse a transimpedance amplifier with a 5-decade range of 1pA to 100nA;
4. Implement a 3 channel PCB that consists of two potentiometric amplifiers and a transimpedance amplifier.

Section 1: Errors at the input and the effects of sensor impedance

To amplify the voltage difference between two electrodes, a differential amplifier is needed. Implementing a single opamp differential amplifier is possible but it results in low input resistance. When the source impedance is high, this produces significant errors.

To mitigate this, two or three opamp topologies are possible (called instrumentation amplifiers or INAs) which guarantee high input impedance by connecting the voltage source directly to an opamp terminal[1]. For better performance and in order to minimize PCB area, INAs can be purchased in packages which contain all components (apart from gain setting resistors). This has the benefit of simplifying the circuit design and analysis through datasheets that describe the complete package specifications.

Before attempting to determine the errors that arise at the INA input, we must discuss an approximate model for the sensor impedance, as well as the non-idealities of the INA.

1. The source will be modelled as two voltage sources (V_1, V_2) with their respective impedances connected to the positive and negative INA terminals. The sensor voltage which is to be amplified is $V_S = V_1 - V_2$, while the common mode voltage is $V_{cm} = \frac{V_1+V_2}{2}$. For the purposes of our analysis, the common voltage will be assumed to be DC.
2. Each of the source impedances (Zs_1, Zs_2) will be approximated by a resistor and a capacitor, in parallel. The two-impedance model captures the effects of mismatch between the two electrodes, while compensating for the simplistic model of each impedance ($Zs_1=Rs_1||C_{S1}$, $Zs_2=Rs_2||C_{S2}$).
3. The INA input impedance will be modelled by a differential input impedance ($Z_d=R_d||C_d$) between positive and negative terminals as well as a common mode impedance ($Z_{CM}=R_{CM}||C_{CM}$) between each terminal and ground[2]. It is assumed that the common-mode input impedance will be the same from each terminal to ground.
4. The INA bias currents will also need to be included. They will be modelled as DC current sources (I_{B1}, I_{B2}) at the INA input terminals. The currents specified in datasheets are the average bias current $I_B=(I_{B1}+I_{B2})/2$ and the offset current $I_O=I_{B1}-I_{B2}$.
5. The input offset voltage will not be included in the model. The resulting error introduced in the output for each gain setting is most often given in the INA datasheet and thus, no further analysis is needed.

[1] Examples in Appendix 1

[2] https://www.analog.com/media/en/training-seminars/tutorials/MT-062.pdf

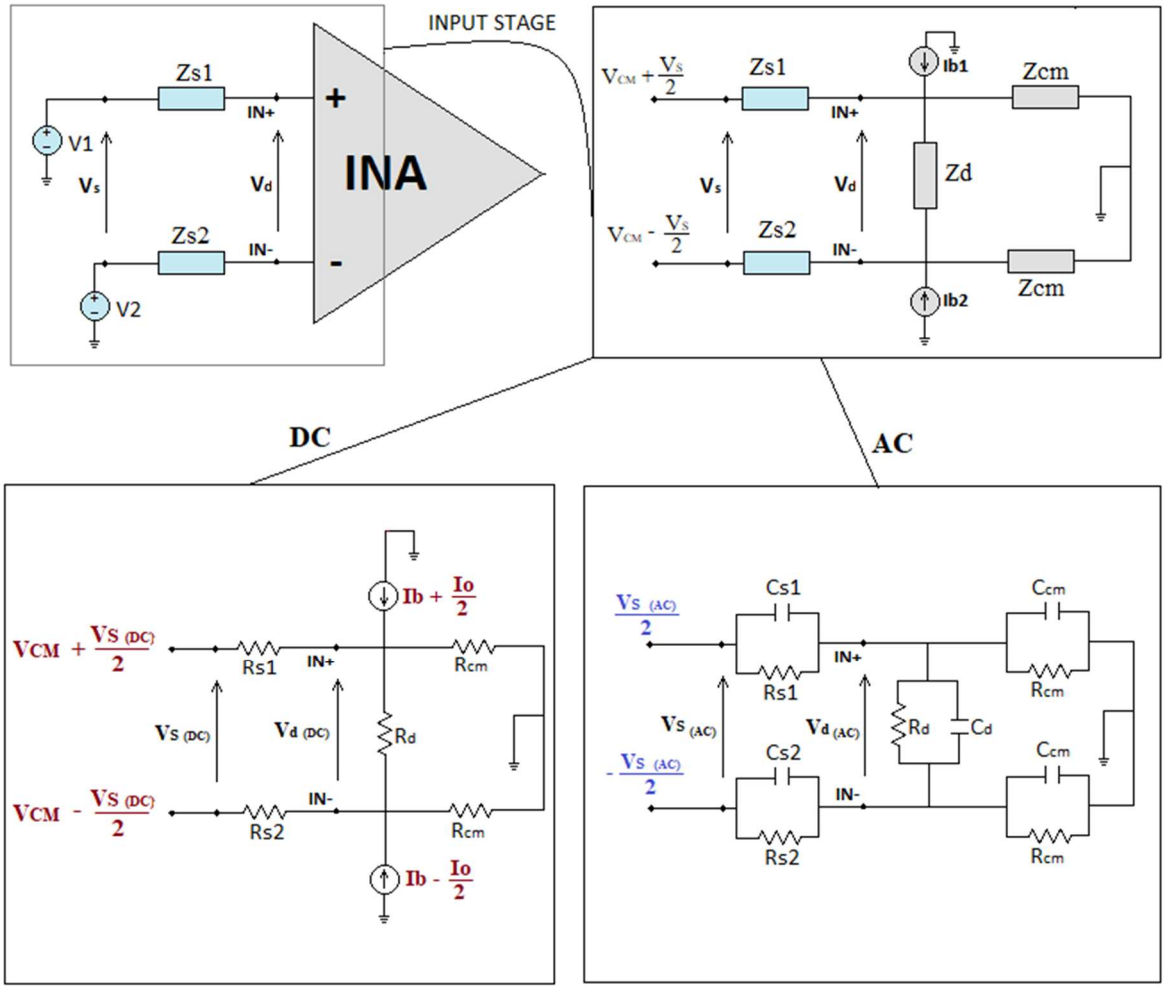


Figure 1. DC and AC model of INA-sensor interface

DC Analysis

KCL@IN+ → $\frac{V_{IN+}-(V_{CM}+\frac{V_S}{2})}{R_{s1}}+\frac{V_{IN+}}{R_{cm}}+\frac{V_{IN+}-V_{IN-}}{R_d}=I_B+\frac{I_O}{2}$

KCL@IN- → $\frac{V_{IN-}-(V_{CM}-\frac{V_S}{2})}{R_{s2}}+\frac{V_{IN-}}{R_{cm}}+\frac{V_{IN-}-V_{IN+}}{R_d}=I_B-\frac{I_O}{2}$

We define $R_{IN} = R_{cm} \parallel R_d$, $\Delta R_S = |R_{s2} - R_{s1}|$ and $Rs_{TOT}=R_{s2} + R_{s1}$. Then, given that $R_{IN}>>Rs_{TOT}$ it can be shown[3] that:

$$\boldsymbol{e_{INPUT_{(MAX)}} = \frac{Rs_{TOT}}{R_{IN}} \cdot V_s + \frac{\Delta R_S}{R_{cm}} \cdot V_{cm} + \Delta R_S \cdot I_B + 0.5 \cdot Rs_{TOT} \cdot I_O}$$

Note that $\frac{Rs_{TOT}}{R_{IN}}$ is the percentage error between V_d and V_s, while the other terms represent an absolute error that will be relatively consistent across all measurements in similar conditions.

[3] Appendix 2 (INA Input DC analysis)

AC Analysis

KCL@IN+ $\rightarrow$ $\frac{V_{IN+}-\frac{V_S}{2}}{\frac{1}{R_{s1}}+s\cdot C_{s1}}+\frac{V_{IN+}}{\frac{1}{R_{cm}}+s\cdot C_{cm}}+\frac{V_{IN+}-V_{IN-}}{\frac{1}{R_d}+s\cdot C_d}=0$

KCL@IN- $\rightarrow$ $\frac{V_{IN-}+\frac{V_S}{2}}{\frac{1}{R_{s2}}+s\cdot C_{s2}}+\frac{V_{IN-}}{\frac{1}{R_{cm}}+s\cdot C_{cm}}+\frac{V_{IN-}-V_{IN+}}{\frac{1}{R_d}+s\cdot C_d}=0$

After enough algebra[4], we can define:

$$G_{IN}(s)=\frac{V_d}{V_s}=\frac{n_2s^2+n_1s+n_0}{d_2s^2+d_1s+d_0}=K\cdot\frac{\left(\frac{s}{z_1}+1\right)\cdot\left(\frac{s}{z_2}+1\right)}{\left(\frac{s}{p_1}+1\right)\cdot\left(\frac{s}{p_2}+1\right)},$$

where K is the DC gain, $p_{1,2}$ are the poles and $z_{1,2}$ are the zeros of the transfer function and all coefficients are functions of the passive components.

Using MATLAB, we sweep through a wide range of combinations[5] of Z_{S1}, Z_{S2}, Z_d, Z_{cm} for frequencies up to 1MHz. We reach two conditions which guarantee that the percentage error $|1 - |G_{IN}(jw)|\,|$ is below a given threshold Er for all ω within a specific frequency range, BW:

$\{\boldsymbol{Rs_{TOT}\cdot C_{IN}\cdot BW<Er}\}$ **or** $\{\frac{C_{IN}}{Cs_{TOT}}<\frac{Er}{a+3},\ \boldsymbol{where\ a=max}(\frac{Cs_1}{Cs_2},\frac{Cs_2}{Cs_1})\}$

Satisfying either of those conditions guarantees that the error is within range throughout the whole signal bandwidth. In the extreme mismatch case $Cs_2 \ll Cs_1$ or $Cs_1 \ll Cs_2$, the second condition becomes impossible to satisfy.

Note that the percentage DC error condition is implied throughout the simulations. In other words, this analysis is only valid once we have verified that $\frac{Rs_{TOT}}{R_{IN}}<Er$!

It is important to recognise that both AC and DC relations that are derived represent the extreme worst possible results. This is of significant importance, as the circuit analysis of a system of known impedances will always allow for more lenient conditions.

[4] Appendix 3 (INA input AC analysis)
[5] Appendix 4 (Simulating INA input)

Finally, it is necessary to specify the boundaries for which the above were simulated and verified to hold true. This is to avoid using these results in the wrong context:

Description	Formula	Simulated Range
Acceptable error	$Er=\|1-V_s/V_s\|$	1% to 10%
INA input resistance	$R_{IN}=R_d \,\|\|\, R_{cm}$	10MΩ to 10TΩ
	$M_{Rin}=R_{cm}/R_{IN}$	1, 10, 100
INA input capacitance	$C_{IN}=C_{cm}+C_d$	1pF to 10nF
	$M_{Cin}=C_{cm}/C_d$	0.1 to 9
Total source resistance	$Rs_{TOT} = R_{s1} + R_{s2}$	10Ω to Er R_{IN}
	$M_{Rs}=R_{s1}/R_{s2}$	0.011 to 99
Total source capacitance	$Cs_{TOT} = C_{s1} + C_{s2}$	1pF to 100uF
	$M_{Cs}=C_{s1}/C_{s2}$	0.011 to 99

Section 2: Amplifiers for potentiometric sensors

In this section, two channels will be designed, each accommodating the characteristics of a different signal. The first channel (Ch1), will amplify and filter bioelectric tissue potential at amplitudes ranging from 50mV to 500mV, with frequencies close to DC (<< 10 Hz). The second channel (Ch2), will amplify the output of a potentiometric sensor. This signal is also effectively DC and ranges from 1mV to 100mV.

	Bioelectric tissue potential	Potentiometric biosensor output
Sensor voltage (V_S)	50mV to 400mV	1mV to 100mV
Common-mode Voltage (V_{CM})	150mV to 300mV	<1V
Bandwidth (BW)	<<10Hz	<<10Hz
Source Resistance	<5MOhm	<50GOhm
Source Capacitance	Unknown	Unknown

As the signals are of same bandwidth and to simplify the process, both channels will be constructed using the same parts. The only difference will be the gain setting resistors, as the gain for Ch1 will be 5 while in Ch2 it will be 20. Then, we can power the amplifiers by ±2.5V, which can be produced from a standard 3.7V battery. In both channels, a 1st order low pass filter will be implemented after amplification, with a cut-off at 10Hz. We will aim for a precision of 1mV at the output (a 1mV step at the input should be detectable).

Before continuing, we need to briefly discuss the amplifier DC offset (V_{OFF}), Common mode rejection ratio (CMRR) and input referred noise.

1. DC offset: The frequency of both signals (~DC), prohibits the filtering of the DC offset. Thus, an error is introduced at the output: $e_{off} = A \cdot V_{off}$, where A is the amplifier gain.
2. Input referred noise: Both signals have bandwidth below 10 Hz. We can therefore use a low pass filter with cut-off at 10Hz after the first amplification stage. This implies that as long as the noise is not enough to saturate the INA (unlikely at the low gain values we are implementing), we are only concerned with 0.1 to 10Hz noise (V_N). This will introduce an error at the output: $e_N = A \cdot V_N$
3. CMRR: Like the DC offset, the frequency of V_S does not allow us to filter the proportion of V_{CM} that reaches the output. This results in $e_{CMRR} = \frac{Vcm}{10^{\frac{a}{20}}}$, where $a = CMRR_{@Gain=A}$

The INA321 by Texas Instruments was chosen for both channels as it fit the specifications necessary for acceptable error:

1. Z_{IN}=10TOhm||3pF

   The high input resistance of 10TOhms allows source resistance up to 50GOhms for 5% error. The input capacitance of 3pF (in practice 10pF due to PCB layout), allows a bandwidth of 0.1Hz with 5% error at 50GOhm source resistance. In cases of very high mismatched resistances, $\frac{\Delta R_S}{R_{cm}} \cdot V_{cm}$ will become significant and should be accounted for through calibration.

2. I_B=0.5pA, I_O=0.5pA

   The sub-picoamp bias currents ensure that even at 50GOhms, the voltage produced across the source resistances will not saturate the amplifier. At such high resistance values, however, the resultant error should be accounted for when calibrating the device.

3. V_{OFF} = 0.2mV

   The offset is significantly below the 1mV precision necessary for our device and is therefore acceptable.

4. V_N=20µV

   The 0.1 to 10 Hz noise is an order of magnitude below the precision.

5. $CMRR_{Gain<25}$=90dB

   As $V_{CM(max)}$ = 1V, the maximum error due to CMRR in the output is 0.03 mV.

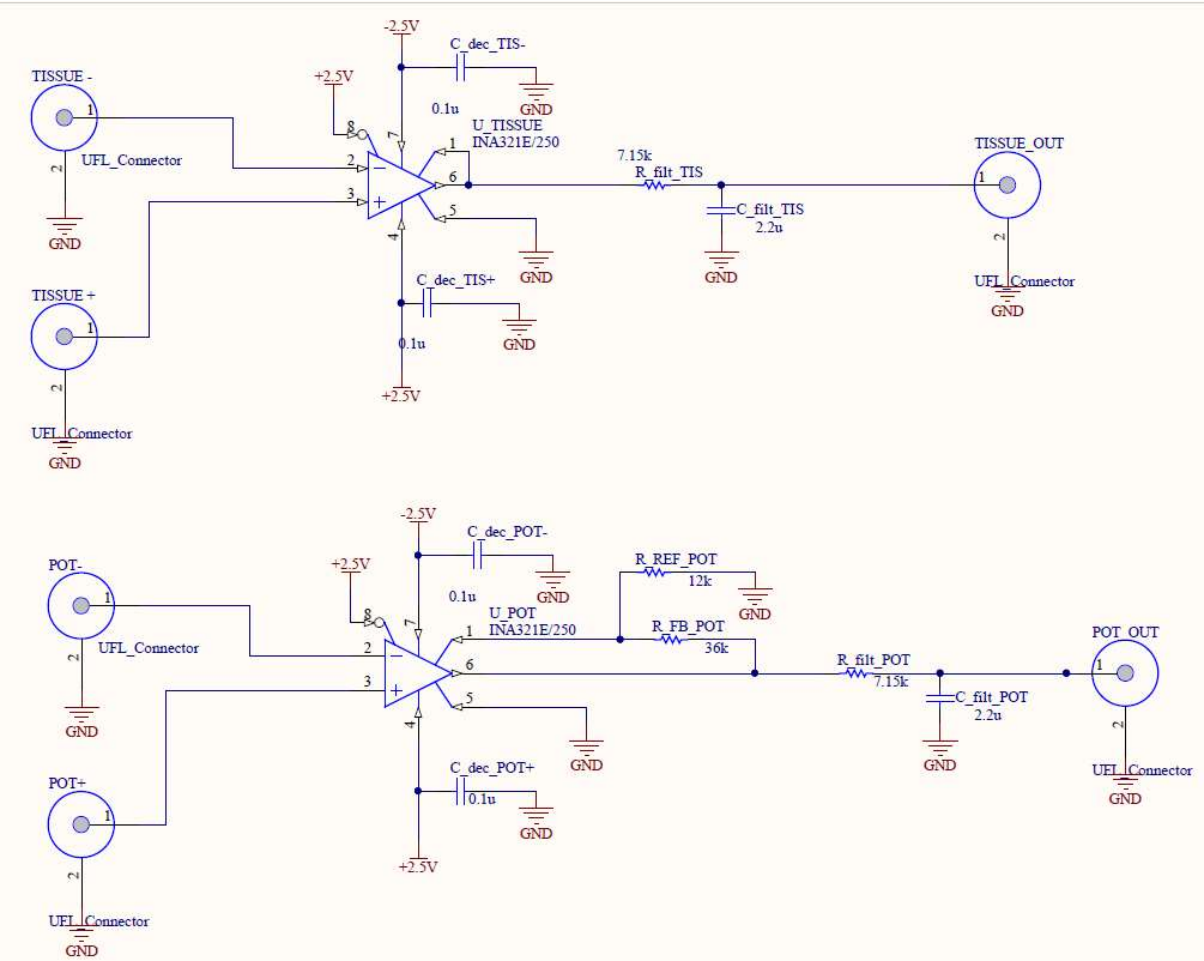


Figure 2. Ch1 and Ch2 complete schematic

Section 3: Transimpedance amplifier for amperometric sensors

In this section, we will discuss the third channel that aims to amplify the current output of an amperometric sensor. The signal has an amplitude range of 1pA to 100nA and is effectively DC. Additionally, the source impedance is in the order of 100s of GOhms. To convert the current to voltage, a transimpedance amplifier must be used.

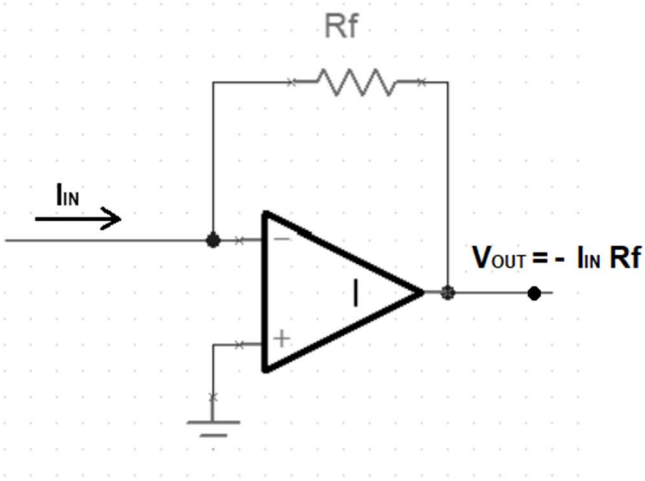


Figure 3. Simple Transimpedance Amplifier

The low current levels to be measured necessitate an amplifier with bias current specifications in the femto-amp range. The LMP7721 by Texas Instruments was chosen for its nominal bias current of 3fA amongst other specifications:

1. I_b=3fA, I_O=6fA, CMRR=100dB

   The bias currents are low enough that they should not hinder the measurement of 1pA currents. CMRR is high enough that any V_{CM} within the amplifier operating limits will not result in significant errors at the output

2. $V_{OFF(MAX)}$=0.5mV

   As the signal is DC, the offset cannot be filtered out. A such, V_{OFF} constitutes the lower bound for the output to the minimum signal (1pA). In other words, a 1pA step should result in an output change larger than 0.5mV. In fact, to be safe we must design the system so that 1pA results in 1mV.

3. Power Supply

   The recommended operating conditions are specified at ±2.5V, which fits well with the designs for Ch1 and Ch2.

4. Open Loop Frequency Response K(s)

   While this is not particularly important for simple designs, it will be necessary to determine in order to assess the stability of the system. To get a decent approximation K(s), we can use the specifications for open loop gain (100dB) and GBW (17MHz). Then, we can say that the DC gain is 10^5 and there will be a pole at ω=2π 170≈1000. Which leads to: $K(s) = \frac{10^5}{1+\frac{s}{1000}}$

Gain Considerations:

Going from 1pA to 1mV implies an amplification of 10^9. However, setting such an amplification will saturate the amplifier at higher current levels (>2.5nA). As such, a switch must be used to change between different gains.

Such a switch must not leak currents larger than 100s of femptoamps. Digital switches cannot provide such low current leakage and manual switches are impractical. A surface mounted reed relay will be used instead. It will be controlled by a digital switch, allowing programmability. The digital part of the design is not within the scope of this report, but it should be relatively simple to program the relay to change its operation whenever the amplifier saturates (thus automating the measuring process).

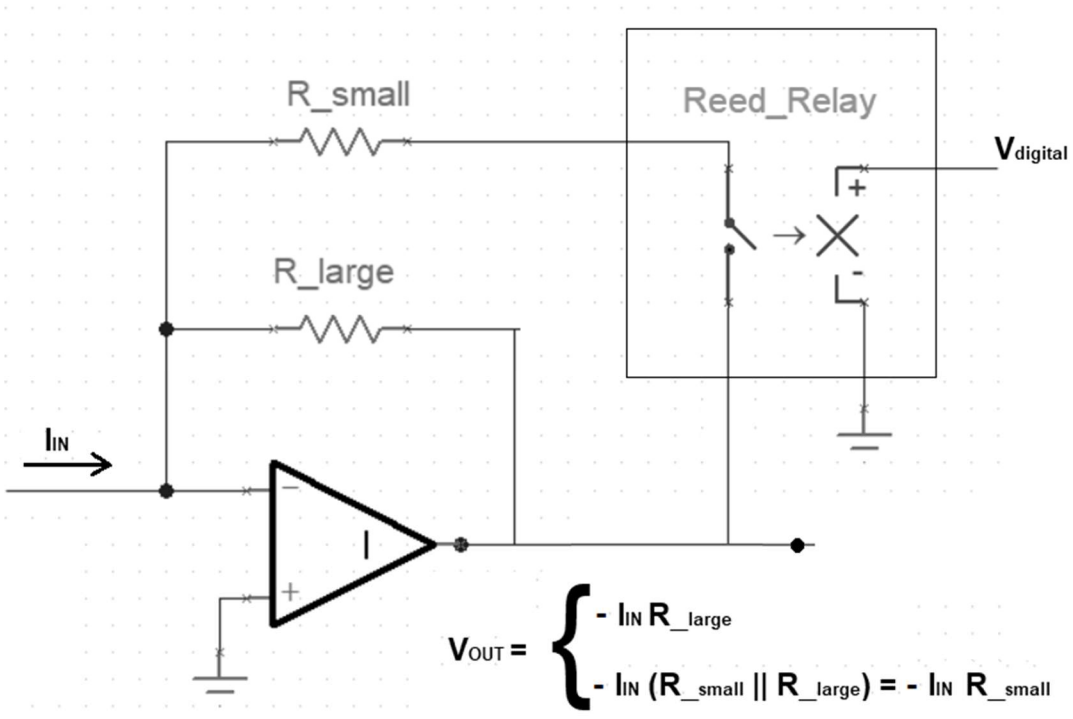


Figure 4. Simplified schematic including reed relay

Resistor values and Relay specifications:

For R_{large}, we will use a 1% tolerance 1GOhm resistor. Larger value resistors are more expensive, larger in size and tend to have higher tolerances. For R_{small}, we want the top of our input current range to map to about 2V. Thus, we choose R_{small}=20MOhm. The parallel combination of R_{small} and R_{large} is 19.6MOhm, an error of 2%.

As the resistance R_{large} is 1GOhm, we select the 9913-series reed relay by Coto Technologies which has R_{OFF} = 100GOhms, R_{ON}<1 Ohm, and 0.25pF effective parallel capacitance. When the switch is off, the parallel combination is 0.99 GOhm, an error of 1%.

Tee feedback:

Having two separate gain settings, allows us to increase the gain for low current levels by implementing a Tee feedback on the loop of R_{large}. This will amplify the voltage drop across R_{large} as well as the input offset voltage and noise. It becomes clear, that this network does not improve precision. It only serves to amplify the signal and allow it to be fed into an ADC without further amplification.

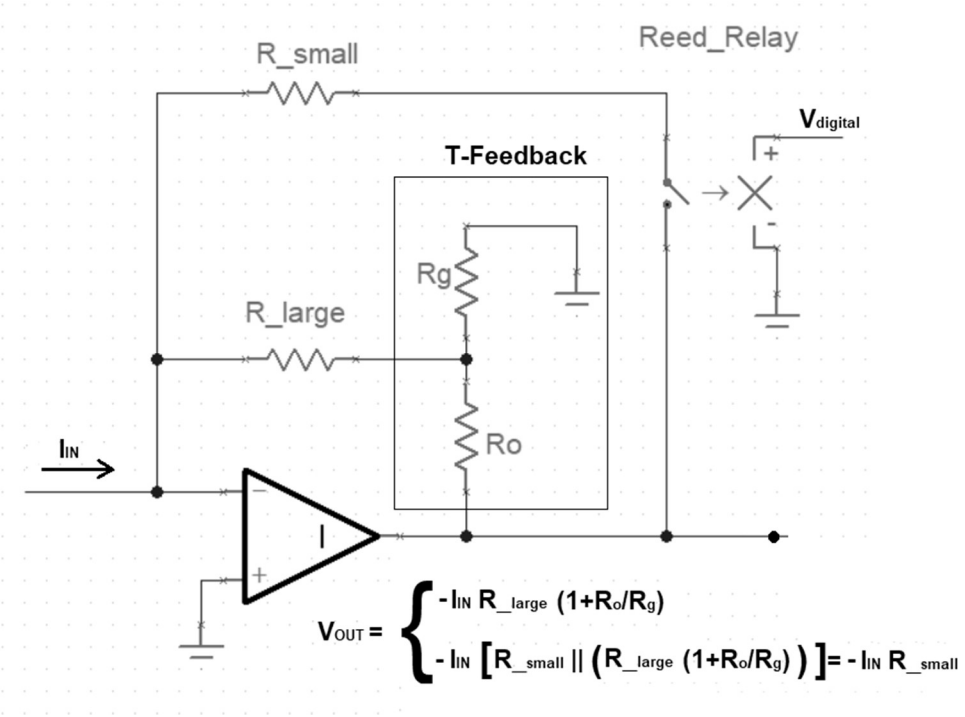


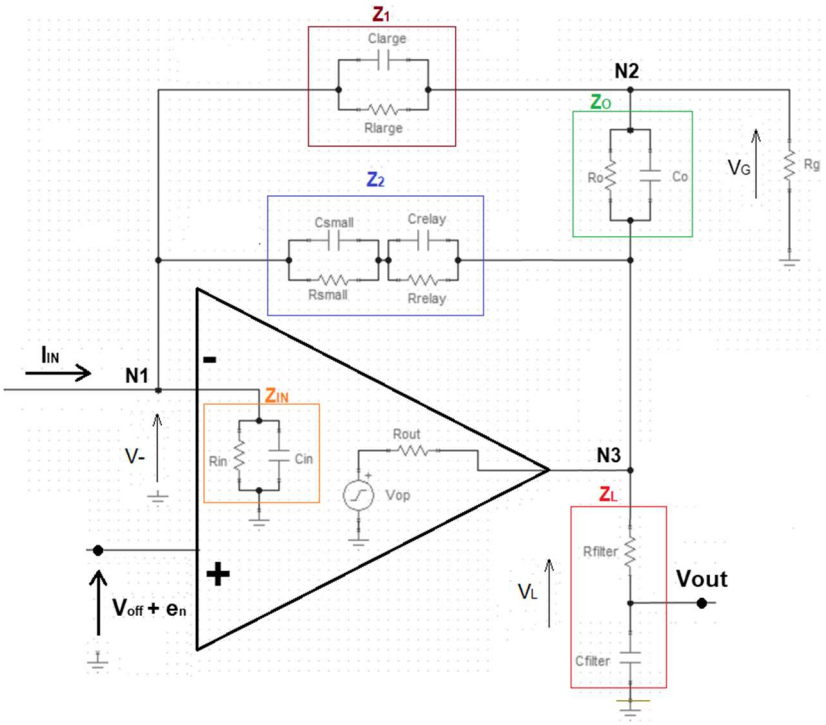
Figure 5. Simplified Schematic including Tee Feedback

We can set R_O/R_G=4, which results in an effective additional gain of 5. By keeping the values of Rg and Ro low enough, we make sure that no additional error is introduced.

Frequency Domain Considerations

We want our system to filter frequencies higher than 10Hz. As such, a 1st order low pass filter will be implemented at the amplifier output. Additionally, by placing capacitors in parallel to R_{large}, R_{small} and Ro we can modify our amplifier to produce additional filtering effects. We also need to check for system stability and choose our capacitor values accordingly.

The LMP7721 does not specify input impedance, input capacitance and output resistance. We will conservatively estimate the parallel combination of the source impedance and the opamp input impedance as 100GOhms and that PCB layout will introduce 15pF of input capacitance. In terms of the output resistance, we will discuss the frequency response for values below 1kOhm.



$R_{IN} = R_{Source} \| R_{IN(LMP7721)} = 100\ G\Omega$
$C_{IN} = 15\ pF$
$R_{Large} = 1\ G\Omega$
$C_{Large} = 16\ pF$
$R_{small} = 20\ M\Omega$
$C_{small} = 820\ pF$
$C_{relay} = 0.25\ pF$
$R_{relay(ON)} = 1\ \Omega$
$R_{relay(OFF)} = 100\ G\Omega$
$R_O = 12\ k\Omega$ (not particularly important as long as $R_O << R_{Large}$)
$R_G = R_O/4 = 3\ k\Omega$ (additional gain: $G_{extra} = 5$)
$C_O = \frac{1}{2\pi R_O \cdot 20} = 0.62\ uF$ ($for\ f > 20Hz, Z_O \to 0 \Rightarrow G_{extra} \to 1$)
$R_{Filter} = 7.15\ k\Omega$ (not particularly important but within specifications)
$C_{Filter} = \frac{1}{2\pi R_{Filter} \cdot 10} = 2.2\ uF$ (1st order low-pass filter with cut-off @10Hz)
The circuit will be examined for $R_{OUT} < 1k\Omega$ and simulated for $R_{OUT} = 100\ \Omega$ and $R_{OUT} = 1k\Omega$

Figure 6. Complete Model

$$V_{OP} = K\left((V_{off} + e_n) - V_-\right)$$

$$V_{OUT} = \frac{1}{1 + s \cdot R_{filt} \cdot C_{filt}} \cdot V_L$$

$$KCL\ @\ N1:\ \ I_{IN} = \frac{V_-}{Z_{IN}} + \frac{V_- - V_G}{Z_1} + \frac{V_- - V_L}{Z_2} \Rightarrow V_- = Z_{P1} \cdot I_{IN} + \frac{Z_{P1}}{Z_1} \cdot V_G + \frac{Z_{P1}}{Z_2} \cdot V_L, \quad where\ Z_{P1} = Z_{IN} \| Z_1 \| Z_2$$

$$KCL\ @N2:\ \ \frac{V_- - V_G}{Z_1} = \frac{V_G}{R_G} + \frac{V_G - V_L}{Z_O} \Rightarrow V_G = \frac{Z_{P2}}{Z_1} \cdot V_- + \frac{Z_{P2}}{Z_O} \cdot V_L, \quad where\ Z_{P2} = Z_1 \| Z_O \| R_G$$

$$KCL\ @N3:\ \ \frac{V_{OP} - V_L}{R_{OUT}} = \frac{V_L}{Z_L} + \frac{V_L - V_G}{Z_O} + \frac{V_L - V_-}{Z_2} \Rightarrow V_L = \frac{Z_{P3}}{R_{OUT}} \cdot V_{OP} + \frac{Z_{P3}}{Z_2} \cdot V_- + \frac{Z_{P3}}{Z_O} \cdot V_G,\ where\ Z_{P3} = Z_L \| Z_O \| Z_2 \| R_{OUT}$$

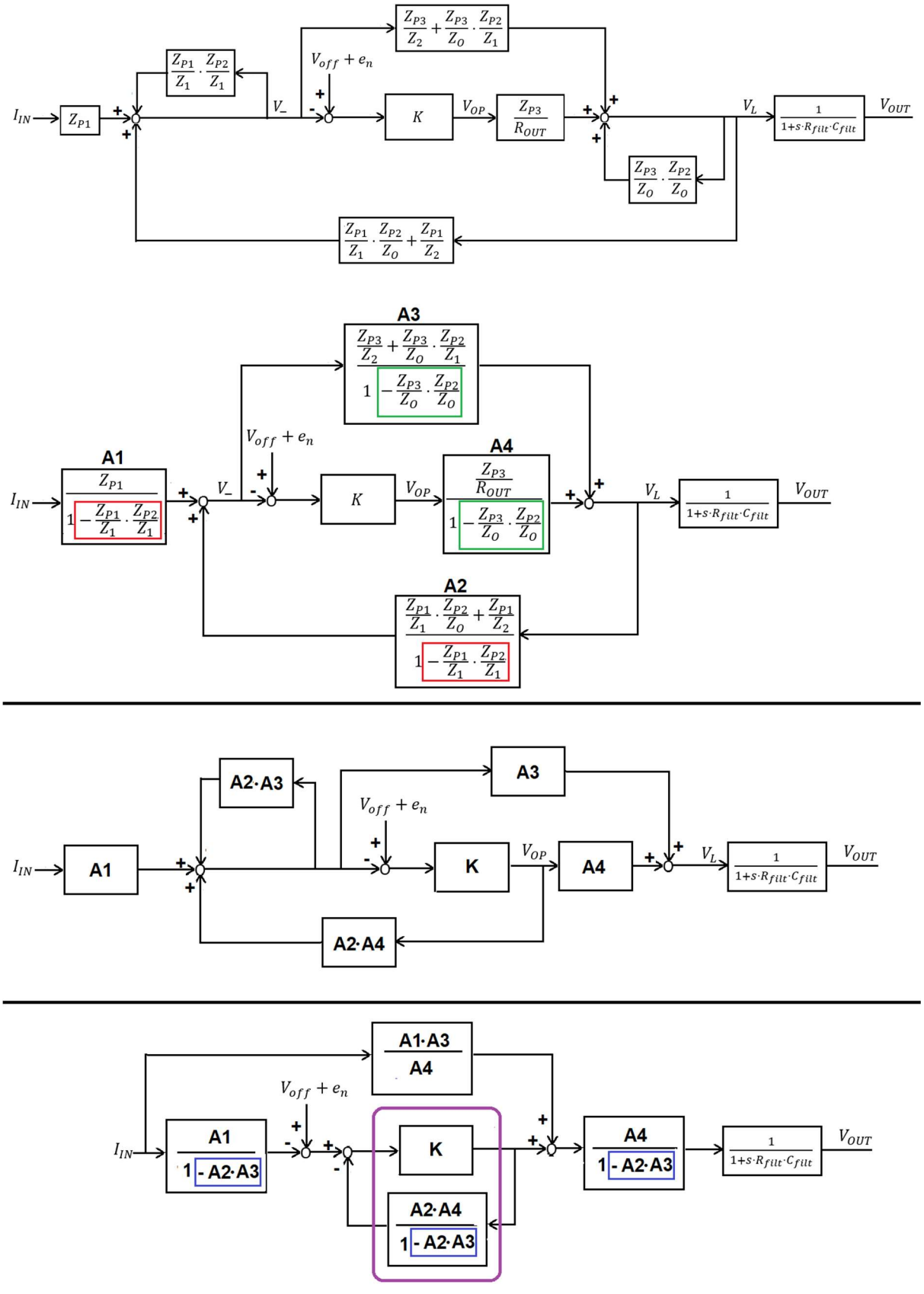
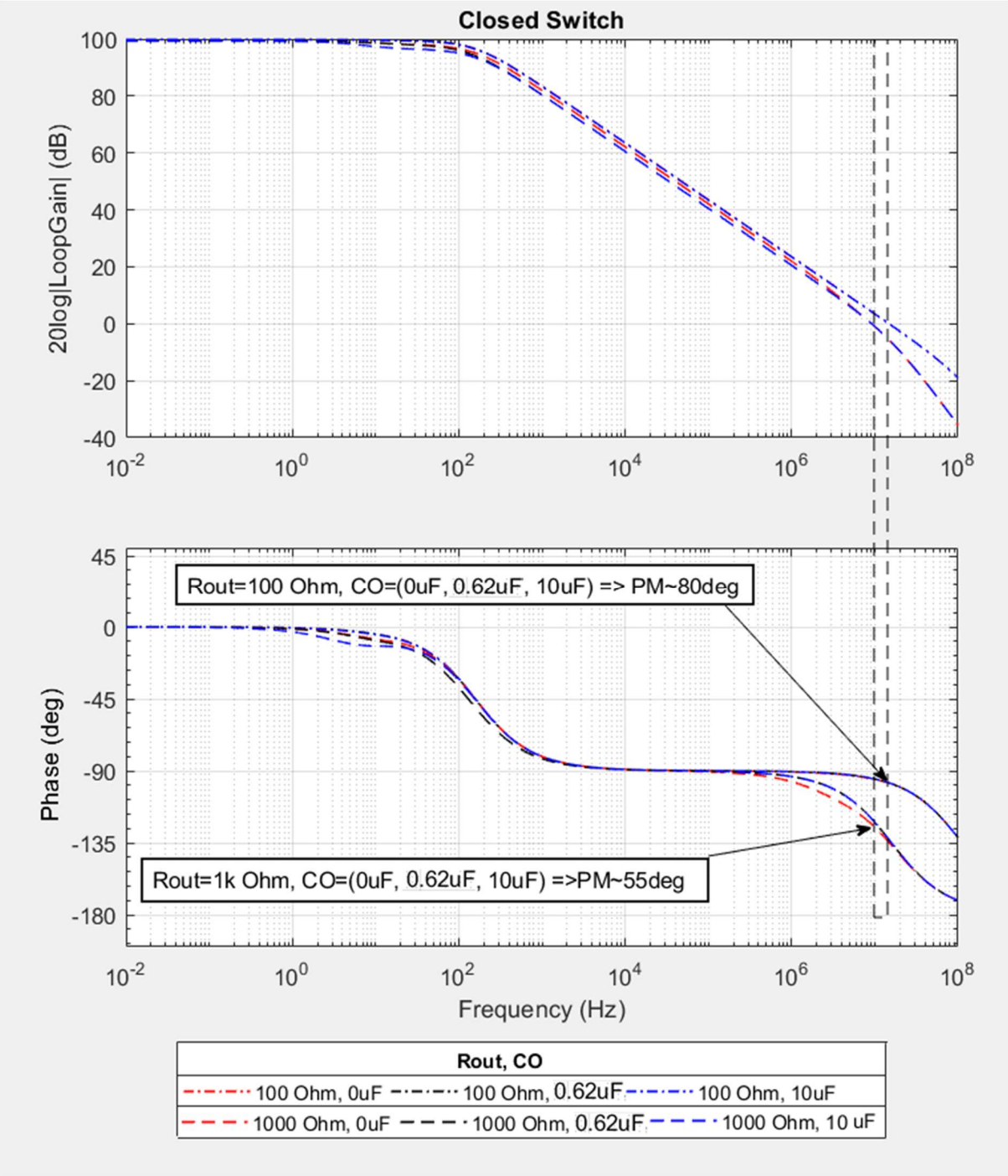


Figure 7. Block Diagram Simplification process
(Highlighting feedback loops that could compromise stability)

Four feedback loops where identified. The minor internal loops (red, green and blue) all have large stability margins[6]. The loop gain, $K \cdot \frac{A2 \cdot A4}{1 - A2 \cdot A3}$, is plotted and the stability margins calculated for R_{OUT} = {100 Ohm, 1k Ohm} and C_O = {0, 0.62 uF, 10 uF}.



[6] Appendix 5 (Transimpedance Minor Loop Stability)

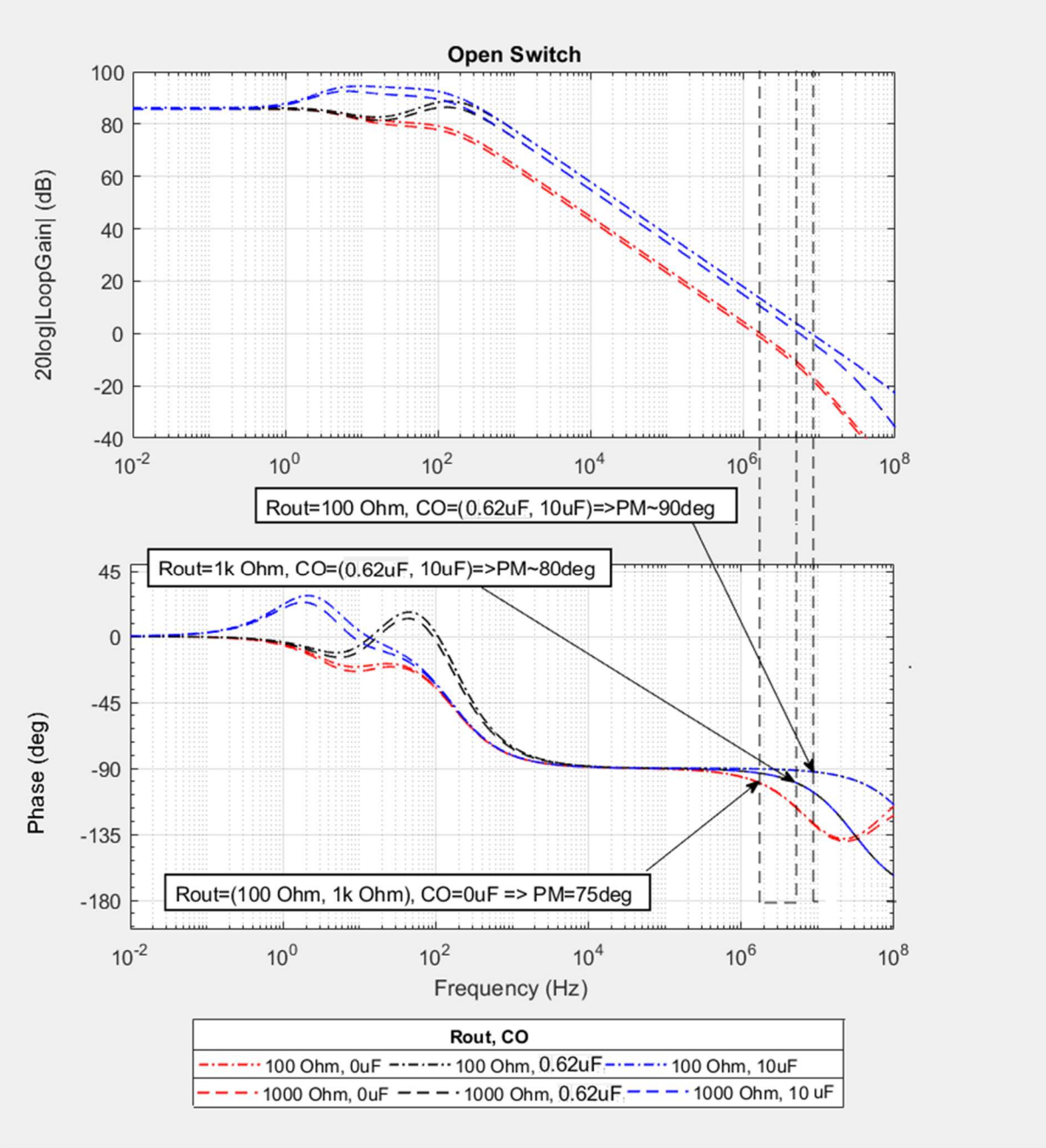


Figure 8. Loop Gain

The loop is stable with PM>45deg in all three cases.

We now plot the frequency response and compare it to a second order low-pass filter with cut-off at 10 Hz. We will plot the normalized gain which allows us to compare the open and closed switch cases effectively.

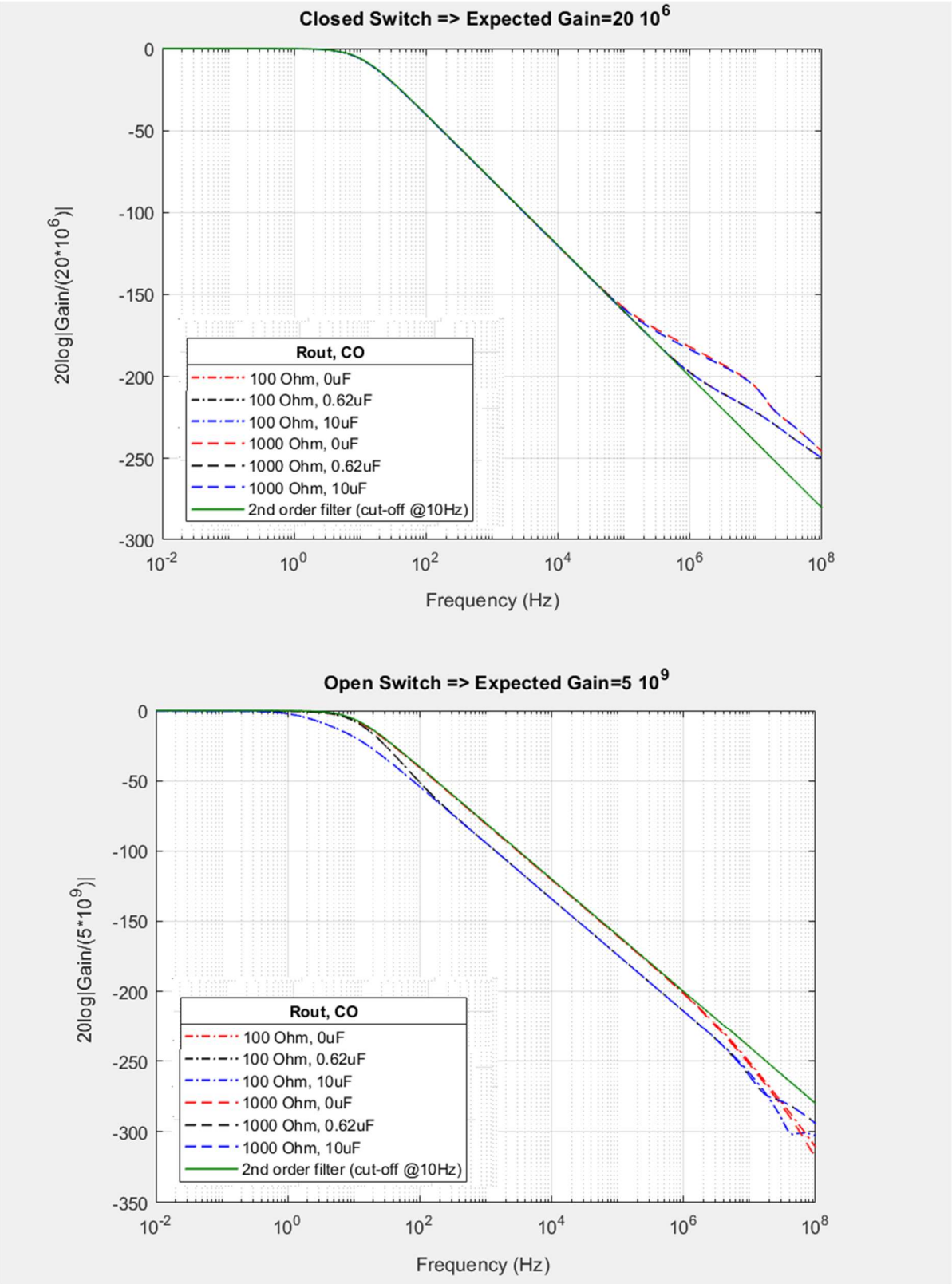


Figure 9. Frequency response of system

From the above plots, it is clear that the gain in the open switch case decreases after the R_OC_O cut-off. To better illustrate this point, we can zoom in to the above graph:

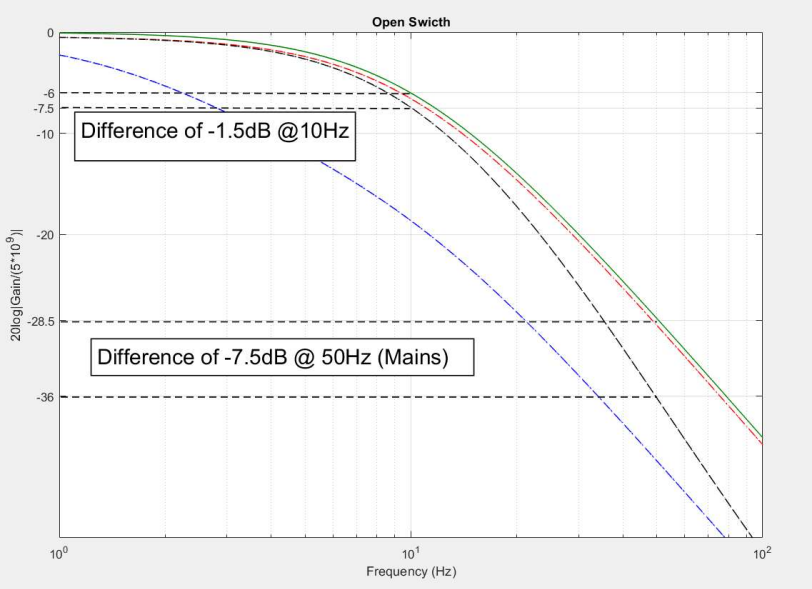


Figure 10. Effects of C_O

Adding the capacitor attenuates the 50Hz frequency by an additional -7.5dB as compared to a 2nd order low pass filter, without attenuating the bandwidth significantly (additional -1.5dB@10Hz).

Finally, we will plot the noise gain of the system and compare it to a 1st order low pass filter with cut-off @10Hz.

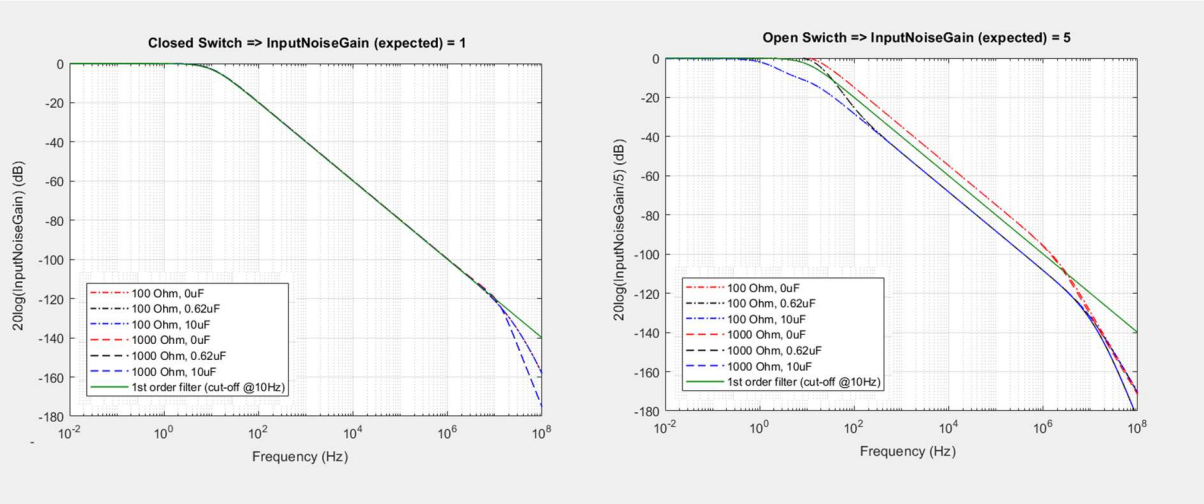


Figure 11. Noise Gain

The noise gain follows the 1st order response closely. It exhibits the same relative attenuation due to C_O as the gain.

Note on Guard rings

When measuring such low current levels, it is often necessary to implement guard rings to prevent current leaking before entering the amplifier loop. These rings are traces that surround the input connectors and input pins of the opamp. These traces are set to the same voltage as the input by means of a buffer amplifier. This prevents current from escaping through the PCB material. This has not been implemented due to time constraints. It would be an improvement on the current design. Nevertheless, care was taken to remove the solder mask around the transimpedance amplifier inputs to minimize leakage.

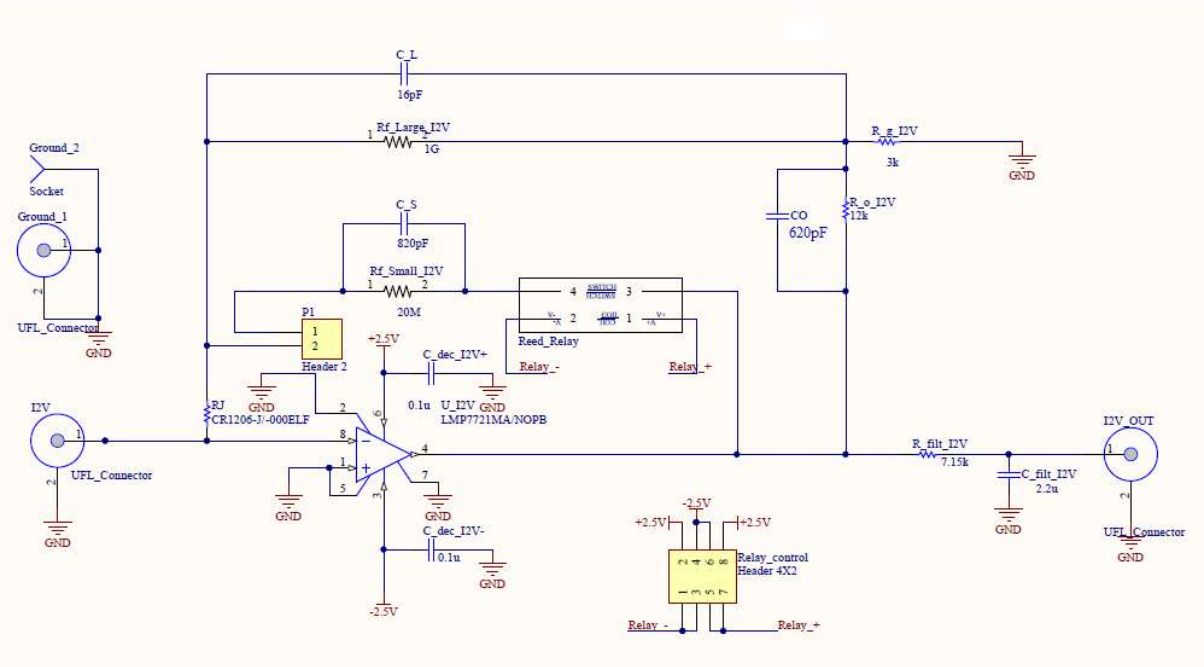


Figure 12. Channel 3 complete schematic

Section 4: Implementation

Power Considerations

All three channels are powered by ±2.5V. To produce both such voltages, the LM27762 LDO is used. This model has the benefit of producing both the positive and negative voltage from a single 3.7V battery. Its low noise specifications and small footprint allow us to use it in a small board (such as the 5cm by 5cm used in this project). Finally, its current output of 250mA is enough to not only power the analog stage designed in this report, but also a modest digital stage.

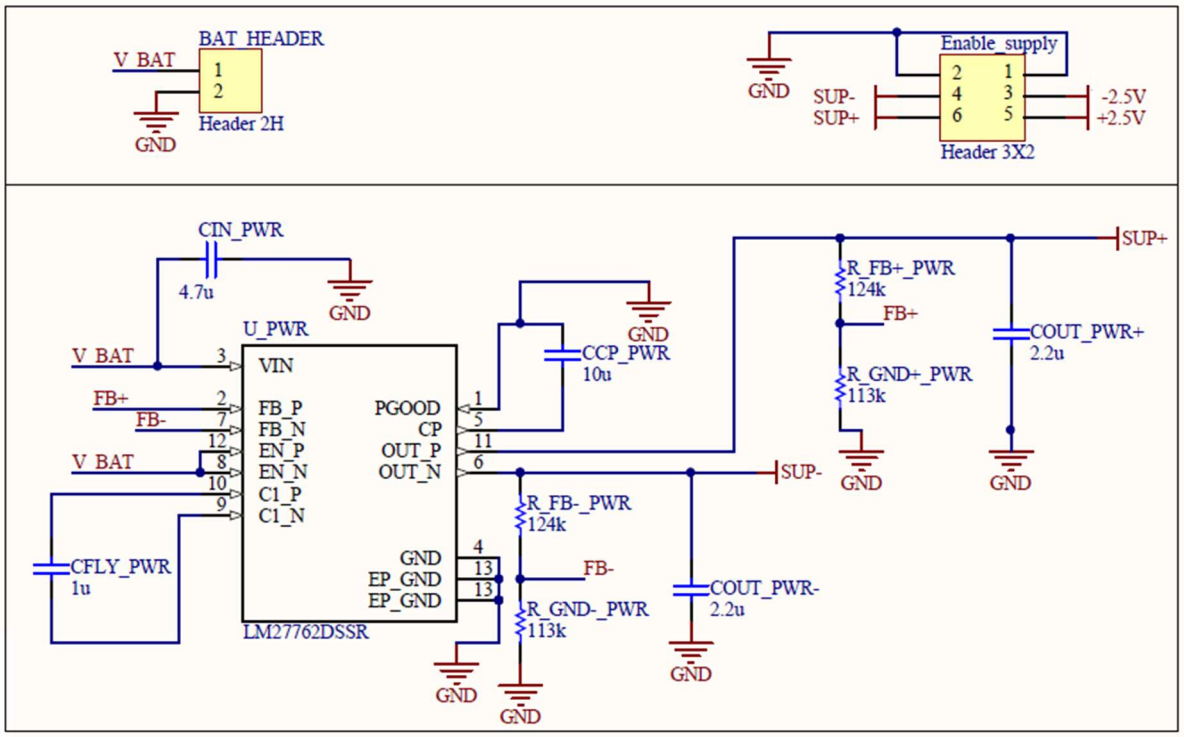


Figure 11. Power Supply Schematic

Overall Structure

The complete 3 channel device was designed to fit on to 5cm by 5cm, 4 layer board, on the Altium Designer© software. The power supply was placed at the furthest point from the analog front end. Additionally, a 2.5cm by 3cm area was left unoccupied to allow for the design of a digital stage.

Board Layout

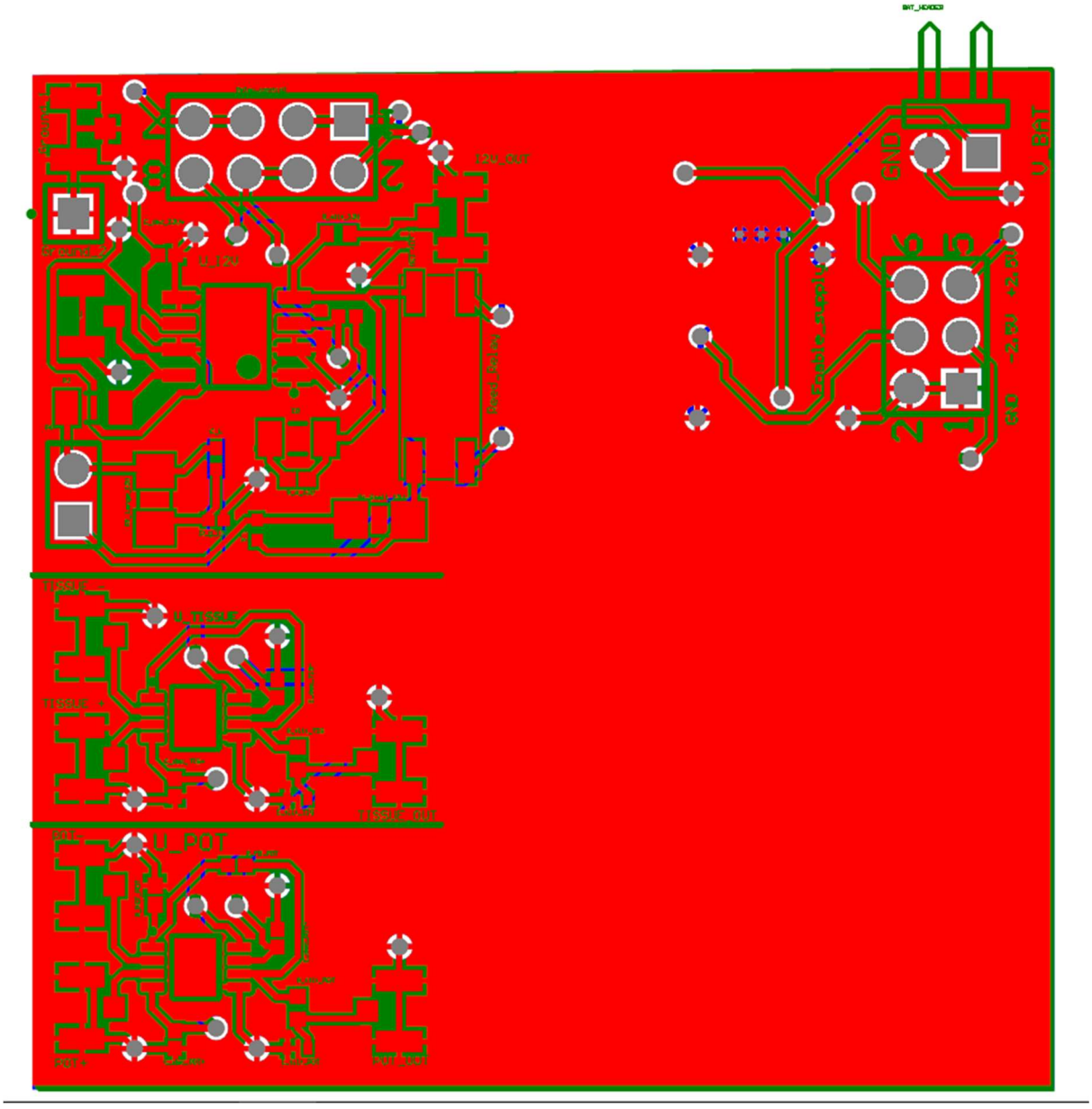
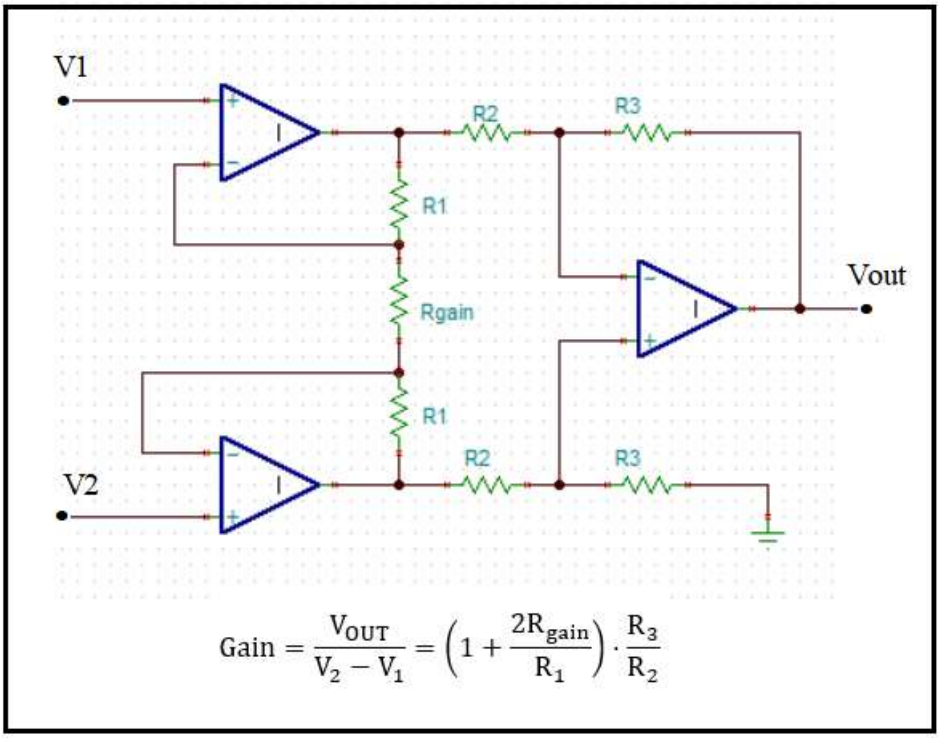


Figure 12. PCB layout

Appendix

1. Simple INA topology examples



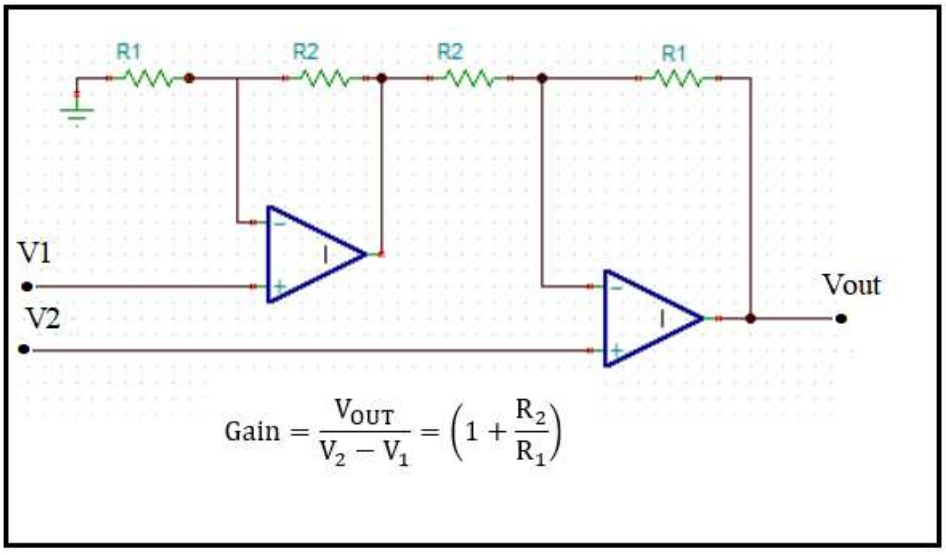


Figure 13. Simple INA topology examples

2. INA Input DC analysis

Define: $r_{s1} = R_{s1}^{-1}$, $r_{s2} = R_{s2}^{-1}$, $r_d = R_d^{-1}$, $r_{cm} = R_{cm}^{-1}$, $r_{p1}=r_{s1}+r_d+r_{cm}$, $r_{p2}=r_{s2}+r_d+r_{cm}$

KCL@IN+

$$\frac{V_{IN+}-(V_{CM}+\frac{V_S}{2})}{R_{s1}}+\frac{V_{IN+}}{R_{cm}}+\frac{V_{IN+}-V_{IN-}}{R_d}=I_B+\frac{I_O}{2} \quad \Rightarrow$$

$$r_{p1}\cdot V_{IN+}-r_d\cdot V_{IN-}=0.5\cdot r_{s1}\cdot V_s+r_{s1}\cdot V_{CM}+I_B+0.5\cdot I_O$$

KCL@IN-

$$\frac{V_{IN-}-(V_{CM}-\frac{V_S}{2})}{R_{s2}}+\frac{V_{IN-}}{R_{cm}}+\frac{V_{IN-}-V_{IN+}}{R_d}=I_B-\frac{I_O}{2} \quad \Rightarrow$$

$$-r_d\cdot V_{IN+}+r_{p2}\cdot V_{IN-}=-0.5r_{s2}\cdot V_s+r_{s2}\cdot V_{CM}+I_B-0.5I_O$$

Hence:

$$\begin{pmatrix} r_{p1} & -r_d \\ -r_d & r_{p2}\end{pmatrix}\begin{pmatrix} V_{IN+} \\ V_{IN-}\end{pmatrix}=\begin{pmatrix} 0.5\cdot r_{s1} & r_{s1} & 1 & 0.5 \\ -0.5\cdot r_{s2} & r_{s2} & 1 & -0.5\end{pmatrix}\begin{pmatrix} V_s \\ V_{CM} \\ I_B \\ I_O\end{pmatrix}$$

$$\begin{pmatrix} V_{IN+} \\ V_{IN-}\end{pmatrix}=\frac{1}{r_{p1}\cdot r_{p2}-r_d^2}\cdot\begin{pmatrix} r_{p2} & r_d \\ r_d & r_{p1}\end{pmatrix}\begin{pmatrix} 0.5\cdot r_{s1} & r_{s1} & 1 & 0.5 \\ -0.5\cdot r_{s2} & r_{s2} & 1 & -0.5\end{pmatrix}\begin{pmatrix} V_s \\ V_{CM} \\ I_B \\ I_O\end{pmatrix}$$

$$V_d=V_{IN+}-V_{IN-}=\frac{1}{r_{p1}\cdot r_{p2}-r_d^2}\begin{pmatrix}1 & -1\end{pmatrix}\cdot\begin{pmatrix} r_{p2} & r_d \\ r_d & r_{p1}\end{pmatrix}\begin{pmatrix} 0.5\cdot r_{s1} & r_{s1} & 1 & 0.5 \\ -0.5\cdot r_{s2} & r_{s2} & 1 & -0.5\end{pmatrix}\begin{pmatrix} V_s \\ V_{CM} \\ I_B \\ I_O\end{pmatrix}$$

We assume that R_{cm}, R_d >> R_{s1}, R_{s2}, then r_{cm}, r_d << r_{s1}, r_{s2}. Now, we can expand and simplify the above:

$$V_d=\frac{1}{r_{s1}\cdot r_{s2}+(r_{s1}+r_{s2})\cdot(r_d+r_{cm})}\begin{pmatrix}V_s & V_{CM} & I_B & I_o\end{pmatrix}\begin{pmatrix} r_{s1}\cdot r_{s2}+0.5\cdot(r_{s1}+r_{s2})\cdot r_{cm} \\ (r_{s1}-r_{s2})\cdot r_{cm} \\ r_{s2}-r_{s1} \\ 0.5\cdot(r_{s1}+r_{s2})+r_{cm}\end{pmatrix}$$

$$e_{IN}=V_s-V_d=\frac{1}{r_{s1}\cdot r_{s2}+(r_{s1}+r_{s2})\cdot(r_d+r_{cm})}\begin{pmatrix}V_s & V_{CM} & I_B & I_o\end{pmatrix}\begin{pmatrix} (r_{s1}+r_{s2})(r_d+0.5\cdot r_{cm}) \\ (r_{s2}-r_{s1})\cdot r_{cm} \\ r_{s1}-r_{s2} \\ -0.5\cdot(r_{s1}+r_{s2})+r_{cm}\end{pmatrix}$$

$$e_{IN} \approx \frac{1}{r_{s1} \cdot r_{s2}} \cdot (V_s \quad V_{CM} \quad I_B \quad I_o) \begin{pmatrix} (r_{s1} + r_{s2}) \cdot (r_d + 0.5 \cdot r_{cm}) \\ (r_{s2} - r_{s1}) \cdot r_{cm} \\ r_{s1} - r_{s2} \\ -0.5 \cdot (r_{s1} + r_{s2}) \end{pmatrix}$$

Define: $R_{IN} = R_{cm} \parallel R_d$ (the definition used by TI for input resistance in their datasheets), $\Delta R_S = |R_{s2} - R_{s1}|$ and $Rs_{TOT} = R_{s2} + R_{s1}$.

Then, the maximum error can be approximated by:

$$\boldsymbol{e_{INPUT_{(MAX)}} = \frac{Rs_{TOT}}{R_{IN}} \cdot V_s + \frac{\Delta R_S}{R_{cm}} \cdot V_{cm} + \Delta R_S \cdot I_B + 0.5 \cdot Rs_{TOT} \cdot I_O}$$

3. INA Input AC analysis

Define: $\zeta_{s1} = R_{s1}^{-1} + s\,C_{s1}$, $\zeta_{s2} = R_{s2}^{-1} + s\,C_{s2}$, $\zeta_d = R_d^{-1} + s\,C_d$, $\zeta_{cm} = R_{cm}^{-1} + s\,C_{cm}$,

$\zeta_{p1} = \zeta_{s1} + \zeta_d + \zeta_{cm}$, $\zeta_{p2} = \zeta_{s2} + \zeta_d + \zeta_{cm}$

KCL@IN+ $\frac{V_{IN+} - (V_{CM} + \frac{V_S}{2})}{\frac{1}{R_{s1}} + s \cdot C_{s1}} + \frac{V_{IN+}}{\frac{1}{R_{cm}} + s \cdot C_{cm}} + \frac{V_{IN+} - V_{IN-}}{\frac{1}{R_d} + s \cdot C_d} = 0 \quad \Rightarrow$

$$\zeta_{p1} \cdot V_{IN+} - \zeta_d \cdot V_{IN-} = 0.5 \cdot \zeta_{s1} \cdot V_s$$

KCL@IN- $\frac{V_{IN-} - (V_{CM} - \frac{V_S}{2})}{\frac{1}{R_{s2}} + s \cdot C_{s2}} + \frac{V_{IN-}}{\frac{1}{R_{cm}} + s \cdot C_{cm}} + \frac{V_{IN-} - V_{IN+}}{\frac{1}{R_d} + s \cdot C_d} = 0 \quad \Rightarrow$

$$-\zeta_d \cdot V_{IN+} + \zeta_{p2} \cdot V_{IN-} = -0.5 \cdot \zeta_{s2} \cdot V_s$$

Hence: $\begin{pmatrix} \zeta_{p1} & -\zeta_d \\ -\zeta_d & \zeta_{p2} \end{pmatrix} \begin{pmatrix} V_{IN+} \\ V_{IN-} \end{pmatrix} = \begin{pmatrix} 0.5 \cdot \zeta_{s1} \\ -0.5 \cdot \zeta_{s2} \end{pmatrix} \cdot V_s$

$$V_d = V_{IN+} - V_{IN-} = \frac{1}{\zeta_{p1} \cdot \zeta_{p2} - \zeta_d^2} \cdot (1 \quad -1) \cdot \begin{pmatrix} \zeta_{p2} & \zeta_d \\ \zeta_d & \zeta_{p1} \end{pmatrix} \cdot \begin{pmatrix} 0.5 \cdot \zeta_{s1} \\ -0.5 \cdot \zeta_{s2} \end{pmatrix} \cdot V_s$$

$$V_d = 0.5 \cdot \frac{\zeta_{p1} \cdot \zeta_{s2} + \zeta_{p2} \cdot \zeta_{s1} - \zeta_d \cdot (\zeta_{s1} + \zeta_{s2})}{\zeta_{p1} \cdot \zeta_{p2} - \zeta_d^2} \cdot V_s$$

$$G_{IN}(s) = \frac{V_d}{V_s} = 0.5 \cdot \frac{\zeta_{p1} \cdot \zeta_{s2} + \zeta_{p2} \cdot \zeta_{s1} - \zeta_d \cdot (\zeta_{s1} + \zeta_{s2})}{\zeta_{p1} \cdot \zeta_{p2} - \zeta_d^2} = K \cdot \frac{\left(\frac{s}{z_1} + 1\right) \cdot \left(\frac{s}{z_2} + 1\right)}{\left(\frac{s}{p_1} + 1\right) \cdot \left(\frac{s}{p_2} + 1\right)},$$

where K is the DC gain, $z_{1,2}$ are the zeros and $p_{1,2}$ are the poles of the transfer function.

4. Simulating INA input

We will use MATLAB to examine G_{IN} and determine the INA input impedance necessary to produce results within our design's error threshold.

Before continuing we need to define the variables used in the simulation as well the range of values spanned for each:

Description	Formula	Simulated Range	Notes
Acceptable error	$Er=\|1-V_s/V_s\|$	1%, 2.5%, 7.5%	Design choice.
INA input resistance	$R_{IN}=R_d \parallel R_{cm}$	10MΩ to 10TΩ	Depends on INA topology and fabrication
	$M_{Rin}=R_{cm}/R_{IN}$	1, 10, 100	While further examination might be useful, M_{Rin} does not appear to affect the maximum error.[7]
INA input capacitance	$C_{IN}=C_{cm}+C_d$	1pF to 10nF	In practice a capacitance of 10pF is likely to appear even for INAs with lower values specified due to PCB layout.
	$M_{Cin}=C_{cm}/C_d$	0.1 to 9	To account for significant capacitance differences due to PCB layout.
Total source resistance	$Rs_{TOT} = R_{s1} + R_{s2}$	10Ω to Er R_{IN}	For Rs_{TOT} > Er R_{IN} the DC error becomes unacceptable.
	$M_{Rs}=R_{s1}/R_{s2}$	0.011 to 99	To ensure that mismatches in source resistance are accounted for.
Total source capacitance	$Cs_{TOT} = C_{s1} + C_{s2}$	1pF to 100uF	To make sure a wide range of sources is covered.
	$M_{Cs}=C_{s1}/C_{s2}$	0.011 to 99	To ensure that mismatches in source capacitance are accounted for.

For each combination (R_{IN}, C_{IN}, M_{Cin}, Rs_{TOT}, M_{Rs}, Cs_{TOT}, M_{Cs}, BW), $|G_{IN}(jw)|$ was computed for values of w ≤ BW. The aim was to determine the range of parameters that allow the whole bandwidth to pass uninterrupted. Success was defined by two conditions:

1. $|G(jw)|<1+Er$ (no unintended amplification anywhere in the bandwidth)
2. $|G(jw)|>|H(jw)|\ (1 - Er)$, where $H(jw)=\sqrt{(1+(w/BW)^2)}$ a 1st order Low pass filter with cut-off at w=BW. This was done to allow slight attenuation at the end of our bandwidth.

By examining the matrix of results, a few key ideas became clear:

1. $|G(jw)|$ is always smaller than 1 for all frequencies observed.

[7] This idea is encouraged by the fact that, while Analog Devices specifies separate values for R_{cm} and R_d, Texas Instruments does not.

2. For each (R_{IN}, C_{IN}, BW) we can define the maximum allowable resistance, Rs_A, that results in no errors for all combinations of the other 4 parameters within our bandwidth. The logarithmic plot of Rs_A vs BW produces the following results:
    a. For BW from DC to some cut-off frequency (defined as cut(R_{IN},C_{IN})), Rs_A =constant > Er R_{IN} (as expected, from the DC analysis).
    b. For BW>cut(R_{IN}, C_{IN}), the slope is equal to -1

Hence, $\log(Rs_A) > \log(ErR_{IN}) + \log\big(cut(R_{IN}, C_{IN})\big) - \log(BW) \Rightarrow \boldsymbol{Rs_A} > \frac{\boldsymbol{Er \cdot R_{IN} \cdot cut(R_{IN}, C_{IN})}}{\boldsymbol{BW}}$

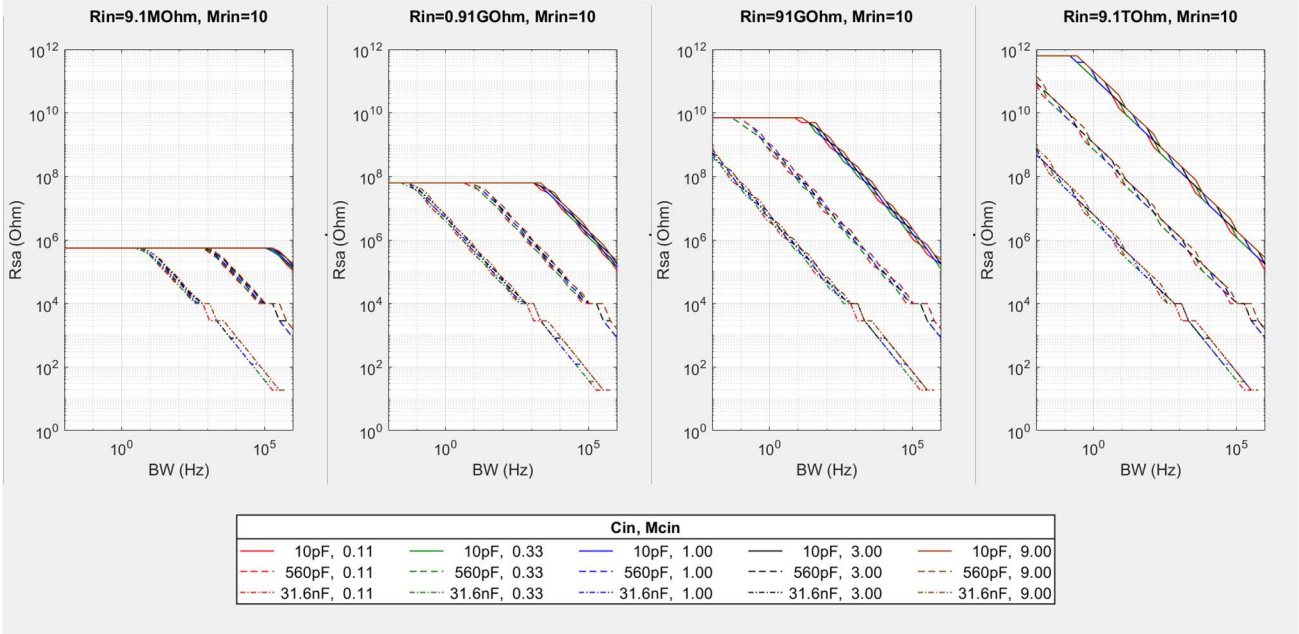


Figure 14. Rs_A (R_{IN}, C_{IN}, BW) vs BW

3. The logarithmic plot of cut(R_{IN}, C_{IN}) vs C_{IN} produces a line of slope -1, as such we can describe $\log(cut(R_{IN}, C_{IN})) = -\log(C_{IN}) + k$. Using linear regression, we determine k for values of R_{IN} within our range, and plot k vs log(Rin). We observe that $-\log(R_{IN}) < k$ for all R_{IN} in our range. Then, we can say that $\boldsymbol{cut(R_{IN}, C_{IN}) > \frac{1}{R_{IN} \cdot C_{IN}}}$.

   Combining the results for 2. and 3. we can say that for any Rs_{TOT}, BW and C_{IN}:

   $\boldsymbol{Rs_{TOT} < \frac{Er}{C_{IN} \cdot BW} < \frac{Er \cdot R_{IN} \cdot cut(R_{IN}, C_{IN})}{BW} \Rightarrow Rs_{TOT} < Rs_A \Rightarrow |G(jw)| \text{ is within error bounds}}$

   This leads us to our first conclusion: Provided the DC percentage error is smaller than Er, if $\boldsymbol{Rs_{TOT} \cdot C_{IN} \cdot BW < Er}$, then at no point within BW will there be error larger than Er.

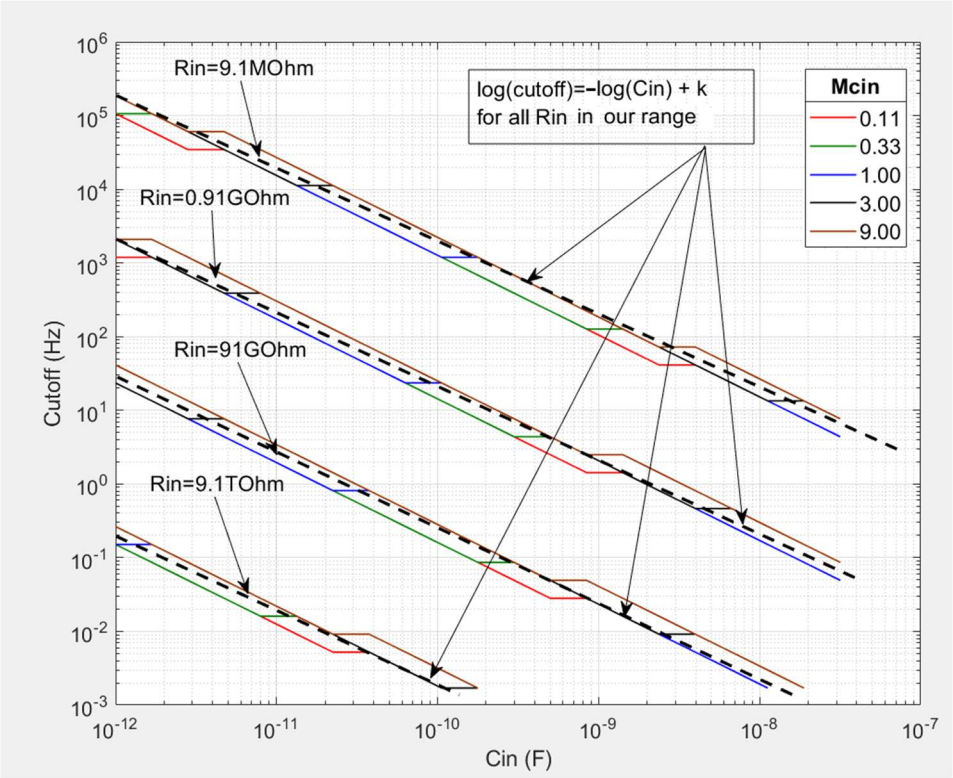


Figure 15. Cutoff vs C_{in}

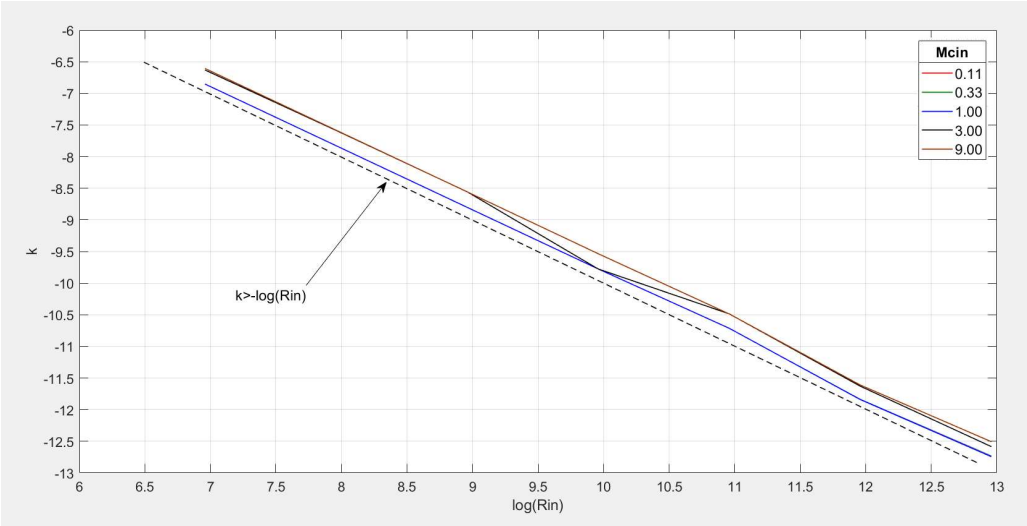


Figure 16. k vs log(Rin)

4. For each (R_{IN}, C_{in}) we define C_{LIM} as the minimum Cs_{TOT} for which success occurs at any frequency (up to 1MHz) for Rs_{TOT} < Er R_{IN} and any combination of the other 2 parameters. The logarithmic plot of $C_{LIM}(R_{IN}, C_{IN})$ vs C_{IN} produces a slope of 1, implying that $C_{LIM} = a \cdot C_{IN}$.

   Hence, we can say that if $C_{IN} < \frac{Cs_{TOT}}{a_{max}}$, success will to occur. This represents the case were the poles and zeros of G_{IN} are within the bandwidth but are close enough together that their effects cancel out.

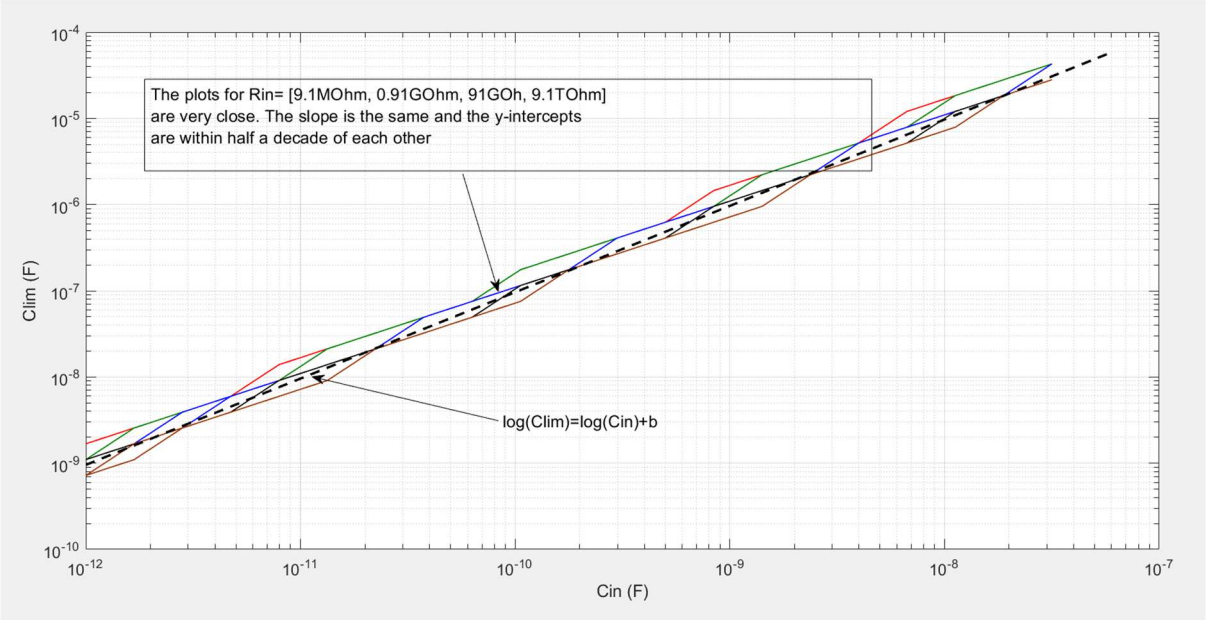


Figure 17. C_{LIM} vs C_{IN}

By examining the coefficients of s^2 in the nominator and denominator of G_{IN} and simplifying them for Cs_{TOT}>>C_{IN} we obtain the relation: $\frac{C_{IN}}{Cs_{TOT}} \cdot \frac{Mc_{IN}+2}{2 \cdot Mc_{IN}+2} \cdot \frac{(Mc_S+1)^2}{Mc_S} < Er$. This can be further simplified by assuming the worst-case, to produce the second condition that guarantees success: $\frac{C_{IN}}{Cs_{TOT}} < \frac{Er}{max(Mc_S)+3}$

Note that this is not a proof, only a hypothesis that fits the simulation results. For the ratio of the coefficients of s^2 to be sufficient to show that the error is within the limits specified, the gain need to be monotonic. If not, then the gain could reach a minimum or a maximum outside our acceptable limits and then tend to a value at infinity that is within bounds.

Using linear regression, we obtain values of a_{MAX} for our three error values and compare the mathematically derived success condition to the one arising from the MATLAB simulation:

Er	$\frac{1}{a_{max}}$	$\frac{Er}{\max(Mc_S)+3}$
1%	$3 \cdot 10^{-4}$	$1 \cdot 10^{-4}$
2.5%	$4 \cdot 10^{-4}$	$2.5 \cdot 10^{-4}$
5%	$6.7 \cdot 10^{-4}$	$5 \cdot 10^{-4}$

The results are in the same order of magnitude $Er/M_{CS} < 1/a_{max}$ in all cases.

In summary: Given Er R_{IN} > Rs_{TOT}, to ensure that $\left|\frac{v_d}{V_s}\right| < 1 - Er$ within a specified bandwidth BW at least one of the following relations must hold:

1. $\boldsymbol{Rs_{TOT} \cdot C_{IN} \cdot BW < Er}$
2. $\frac{\boldsymbol{C_{IN}}}{\boldsymbol{Cs_{TOT}}} < \frac{\boldsymbol{Er}}{\boldsymbol{Mc_S+3}}, \boldsymbol{where\ Mc_S = max(\frac{Cs_1}{Cs_2}, \frac{Cs_2}{Cs_1})}$ $\boldsymbol{(the\ mismatch\ parameter)}$

5. <u>Transimpedance Minor Loop Stability</u>